# Sensing Voltage Transients Using Built-in Voltage Sensor

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## ABSTRACT

Voltage transient is a kind of voltage fluctuation caused by circuit inductance. If strong enough, voltage transients can cause system failure or permanent hardware damage. To effectively measure voltage transient is a undergoing research topic for many research institutes and high-tech companies, but not many sensors are successfully developed. Also, the characteristics of voltage transient like time scale, frequency and amplitude are not fully understood. To better study the voltage noise characteristics of modern ICs, in this project we investigate a new purely digital voltage sensor that can detect voltage transients timely and effectively. We choose suitable delay elements for different part of our design, and work out a complete voltage sensor. Also we perform several simulations using our sensor, showing that our design can effectively measure voltage transient in our modeled network work.

**Key words**: voltage transient, delay line, TDC, buffer, open latch, Edge shifting

## 1. INTRODUCTION

As the feature size of modern integrated circuits is continuously shrinking, the voltage safe margin of state of the art electronic systems is increasingly being tightened. During operation, changes in system activities inevitably cause voltage fluctuations. Due to circuit inductance, current changes in the circuit can cause supply voltage to fluctuate. Other factors like IR drop also contribute to voltage noises in modern ICs. The voltage fluctuation caused by circuit inductance is called voltage transient. If strong enough, voltage transients can cause large swings of supply voltage to bring supply voltage below nominal value (undershoot), which may cause function failures in the system, or above nominal value (overshoot), which may cause permanent hard damage to the system.

Voltage transients often happen when one part or some parts of the circuit suddenly begin to work or stop to work, causing large current changes which further cause voltage changes. As modern processors become increasingly complex and some low power techniques, such as power gating and clock gating, are used, voltage transient is an important factor that deteriorates the voltage safe margins of these modern processors, limiting their nominal voltage far above the minimum to avoid the worst case conditions.

Although voltage transient is a known problem, its characteristics remains unclear. Previous work [1] [3] in this area is limited. Questions like how fast does voltage transient happen, what are its frequency and amplitude are interesting to researchers. To answer these questions, a voltage sensor able to effectively sense voltage noise is needed. To facilitate the study of voltage noise characteristics of modern ICs, in this project we will investigate a new purely digital voltage sensor that can detect voltage transients timely and effectively. Our voltage sensor consists of two key components: a delay line that senses voltage noises and converts them to delays, and a time to digital converter (TDC) that converts the delay to binary digital code. We will build the voltage sensor using the FreePDK 45nm technology and evaluate its resolution, performance and overhead using. We will simulate the voltage sensor and layout it in the project.

The ability to effectively sense voltage noises is very useful in modern ICs. The voltage sensor could be used to detect voltage glitch attacks (an attacker causes voltage glitches in a system and steal secret information from the faulty information) [4], or used to sense voltage fluctuations to indicate the voltage safe margin of a system, such as the IBM critical path monitor [2]. In the project, we will also explore the potential application of the proposed voltage sensors. Some of the areas where the voltage sensor may be used include: security where the voltage sensor can detect any voltage related attacks or the voltage noise could be used to produce random numbers, voltage safe margin monitoring, testing purposes where the voltage sensor could be used to test the noise levels within an IC.

## 2. Related Work

In many scientific areas, measuring small time intervals is very helpful and necessary. In a digital system, time is measured using clock cycles. However, when there is a need to measure time smaller than one clock cycle, traditional time measuring technique is no longer useful. A time-to-digital converter can measure time scale that is far less than one clock cycle in a digital system, fulfilling needs of measuring time within one clock cycle.

There are many architectures of implementing a time-to-digital converter. The key idea of time-to-digital converter is a delay line with many delay elements that can divide time into small sections, represented by the delay of each delay elements. One time-to-digital architecture using delay line of buffers is shown in Figure 1 [1].

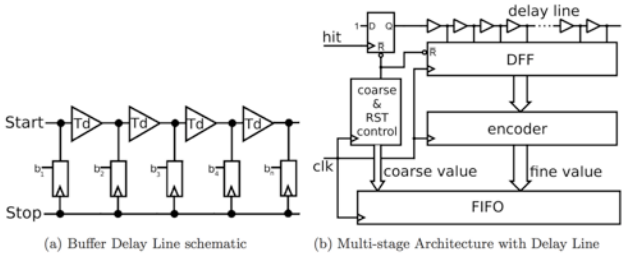


**Figure 1. A time-to-digital converter using delay line**

In this architecture, a start signal is fed into the delay line first and then a stop signal is sent to sample the state of the delay line. By the time the stop is sent, the start already propagates to some point of the delay line, making the first half of the delay elements in high voltage and the other half in low voltage. The flip-flops sample the state of the delay line and output a sequence of binary digital code, for example “11110000”, from which time within a

clock cycle can be interpreted. The resolution of the TDC is determined by the delay of each delay element.

Microprocessor voltage levels include substantial margin to deal with process variations, voltage noises, workload induced thermal and voltage variation, random uncertainty and test inaccuracy. While enough margin can ensure that the processor always work safely even under the worst cases, most of the time the process is not suffering from the worst cases and could operate at a much higher frequency. To deal with this problem, a Critical Path Monitor is proposed in [2] to exploit the often larger than necessary voltage margin to save power or boost processor performance. The CPM monitors the time margin of a critical path on the processor to indicate whether the processor should be operated faster or slower. Figure 2 shows the CPM and its application in a processor core. The key component of the CPM is actually the time-to-digital converter. An input signal is fed into the delay line of a time-to-digital converter and the flip-flops sample the state of the delay line at the arrival of another signal, which can be the clock. The time-to-digital converter is calibrated so that under nominal voltage the input signal always propagates to the middle of the delay line when the sampling signal arrives. When the system voltage is higher than the nominal voltage, the delay of the delay line is smaller and the input signal propagates further in the delay line, indicated by a right shift of the edge of the digital binary code. When the system voltage is lower than the nominal voltage, the delay of the delay line is larger and the input signal propagates shorter in the delay line, indicated by a left shift of the edge of the digital binary code. The control part of the processor monitors the edge of the digital binary code and tells the clock generator to speed up or slow down to better adapt to the system safe margin.

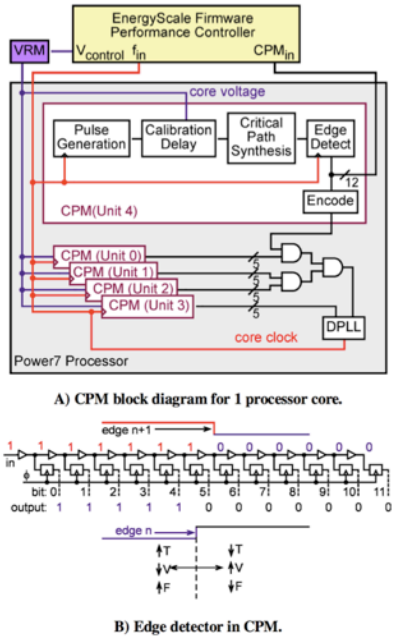


**Figure 2. IBM Critical Path Monitor**

Many industrial state of the art ICs can sense voltage at various locations on the die and at speeds high enough to detect voltage transients within short time scale. An example is the voltage droop detector proposed by Intel in [3]. The detector circuit proposed consists of 1) an analog front end that samples the voltage of the local power supply and 2) digital control logic. Figure 3 shows the block diagram of the voltage droop detector. The core component of Intel's voltage droop detector is the Analog Digital Converter (ADC). The ADC is directly connected to the power grid to convert the analog voltage signal to digital code. The control block manages the interface to the ADC block, process data from the ADC, and manage the scan-based interface to the processor. High and low "watermark" values are stored to indicate the largest and smallest values detected. The droop detector was tested and the results corresponded to oscilloscope measurement.

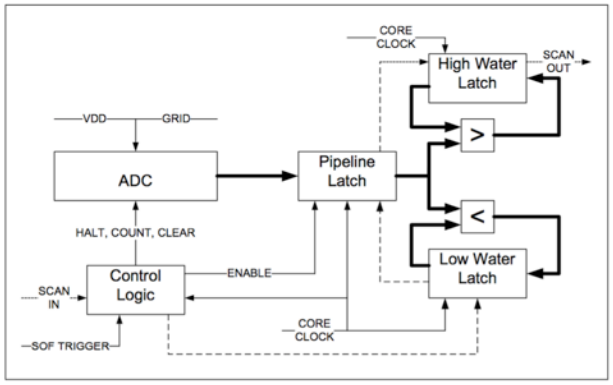


**Figure 3. Intel voltage droop detector circuit block diagram**

In [4], IBM proposed using similar delay line to measure clock jitter and clock skew. The architecture is shown in Figure 4. Unlike the delay elements used in our design, the SKITTER sensor proposed in [4] uses a single inverter as the basic delay element. The design also uses latches to sample the voltage on the delay line. Instead of getting a sequence of '1' or '0', the SKITTER gets a sequence of "10". If there happens to be large jitter or clock skew, abnormal bits like "11" or "00" will appear in the digital code. The circuit that captures the edge is shown in the following figure. A clock splitter splits the global clock into two so that at each rising and falling edge of the clock the latch can sample one time at each of the events. Besides measuring the jitter and SKITTER sensor also takes into account the effect of voltage changes on the clock jitter and skew, because the delay line is very sensitive to voltage changes and it also reflect voltage changes.

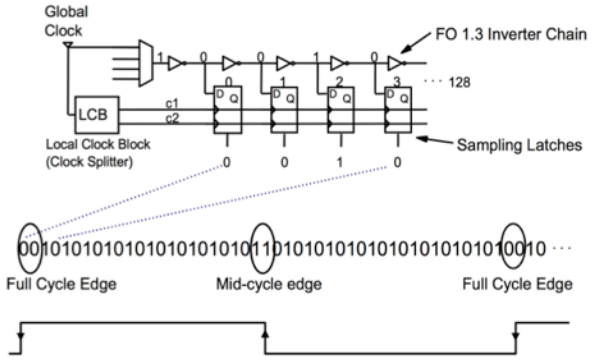

**Figure 4. IBM SKITTER sensor.**

## 3. Design of the Voltage Sensor

To facilitate the study of the voltage transients, a voltage sensor that can effectively sense the voltage changes is desired. In this section, we will present our voltage sensor which is purely digital and able to effective sense the voltage fluctuations. Our voltage sensor consists of two key components: a voltage sensitive delay line and a Time to Digital Converter (TDC). The voltage sensitive delay line is used to sense the voltage fluctuations and convert the voltage fluctuations into timing delay. The TDC is used to convert the timing delay into a sequence of digital code which indicates the voltage level.

### 3.1. Design Specifications

Before beginning the design of the sensor, some specifications of the sensor are set. Our design is based on the 45nm FreePDK library, and the nominal voltage in this library is 1.1V. We hope our sensor can detect voltage changes as small as 10mV, and the sensor can work in the voltage range of 0.8V to 1.4V. The sensor outputs a digital code of 64 bits. Every bit shift in the digital code corresponds to 10mV voltage change, thus the resolution of the sensor is 1bin/10mV and the measuring range of the sensor is 640mV. Here "bin" is used to indicate one binary digit. The design specifications are shown in Table 1.

**Table 1. Design specification of the voltage sensor.**

| Minimum voltage | Nominal voltage | Maximum voltage | Resolution | No. of bins | Range |
|---|---|---|---|---|---|
| 0.7 V | 1.1 V | 1.5 V | 1 bin/10mV | 64 | 640mV |

### 3.2. Voltage Sensitive Delay Line

The voltage sensitive delay line is a sequence of delay elements which are sensitive to voltage changes. In this project, we tested three basic delay elements (buffer, open latch and transmission gate), and tend to choose the one with the highest sensitivity to voltage changes for this part of design. In order to test the delay of each of the elements listed above, we use two same elements in every testing, one as the load of the other one which is tested. Following the design specification mentioned in 3.1, we have the following results in table 2, 3 and 4.

**Table 2. Voltage-delay profile of a buffer**

| voltage (V) | rising time (ps) | falling time (ps) | tp (ps) |
|---|---|---|---|
| 0.7 | 40.7 | 40.6 | 40.75 |
| 0.8 | 35.5 | 34.6 | 35.15 |
| 0.9 | 21.8 | 35.3 | 34.05 |
| 1.0 | 29.6 | 29.9 | 29.75 |
| 1.1 | 29.3 | 26.6 | 28.95 |
| 1.2 | 29 | 28.3 | 28.65 |
| 1.3 | 27.2 | 27.6 | 27.4 |
| 1.4 | 26.7 | 27.6 | 27.15 |
| 1.5 | 25 | 26 | 25.5 |

**Table 3. Voltage-delay profile of a transmission gate**

| voltage (V) | rising time (ps) | falling time (ps) | tp (ps) |
|---|---|---|---|
| 0.7 | 31.6 | 33.2 | 32.4 |
| 0.8 | 25.8 | 30.3 | 28.05 |
| 0.9 | 27.4 | 34.7 | 31.05 |
| 1.0 | 25.4 | 31 | 28.2 |
| 1.1 | 26.4 | 29.7 | 28.05 |
| 1.2 | 23.7 | 30.4 | 27.05 |
| 1.3 | 23.7 | 28.7 | 26.2 |
| 1.4 | 23.1 | 27.1 | 25.1 |
| 1.5 | 22.1 | 26.7 | 24.4 |

**Table 4. Voltage-delay profile of an open latch**

| voltage (V) | rising time (ps) | falling time (ps) | tp (ps) |
|---|---|---|---|
| 0.7 | 100.1 | 99.79 | 99.945 |
| 0.8 | 78.5 | 80.05 | 79.275 |
| 0.9 | 80.4 | 77.87 | 79.135 |
| 1.0 | 69.7 | 70.35 | 70.025 |
| 1.1 | 70 | 68.31 | 67.805 |
| 1.2 | 67.3 | 68.31 | 67.805 |
| 1.3 | 64.4 | 61.9 | 63.25 |
| 1.4 | 59 | 66 | 62.5 |
| 1.5 | 60.6 | 62.36 | 61.48 |

A comparison plot is shown in figure 5:

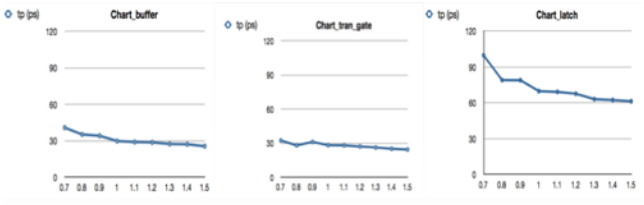


**Figure 5. Voltage-delay comparison between buffer, transmission gate and open latch**

From this figure, it can been seen that all the three basic delay elements have similar voltage-delay relationship, that is the delay decreases as the voltage increases. However, they also have significant difference. The delay of the open latch is about twice the delay of the buffer or the transmission gate under the same voltage. In addition, the open latch is more sensitive to voltage changes, as can be seen in the figures that the slope of the voltage-delay curve of the open latch is steeper than that of the buffer or the transmission gate. This is very useful in that we can use the open latch as the delay line that senses the voltage changes, and use the buffer as the delay elements in the TDC. This is because that the delay line is the key component that senses the voltage changes and it is required to be as more sensitive as possible, and the delay element in the TDC is used to convert delay to voltage and it is required to be as less sensitive to voltage as possible. Also we choose buffer over transmission gate because that extra buffer should be added when using transmission gate in order to separate input from output, which is an obvious drawback. based on the pervious tests and analysis, we use buffer as the delay element in the TDC and use open latch as the delay element in the delay line. The sensitivity of the buffer and the open latch is calculated and shown in Table 5.

**Table 5. Sensitivity of the buffer and open latch**

| | number of transistors | delay/voltage |
|---|---|---|
| **buffer** | 4 | 1.333ps/100mv |
| **latch** | 8 | 2.542ps/100mv |

The delay line consists of a number of open latches as the basic delay elements. The schematic of the delay line is shown in Figure 6 and Figure 7. Figure 6 shows a delay line of only 10 delay elements, and a delay line of 100 delay elements consists of 10 delay line with 10 delay elements. This is to save the workload of drawing the delay line schematic.

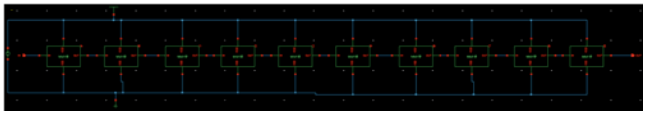

**Figure 6. A delay line with 10 delay elements**

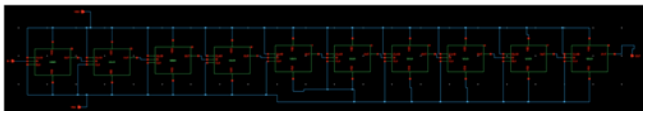

**Figure 7. A delay line with 10 delay lines with 10 delay elements**

## 3.3. Time to Digital Converter

Some analysis about the delay elements in TDC is included in 3.2. The delay element used in the TDC is the buffer, which is not that sensitive to voltage changes compared with the open latch. Flip-flops are used to sample the delay elements. A schematic of the TDC with 8 bins is shown in Figure 8 and a schematic of the TDC with 64 bins is shown in Figure 9. The TDC with 64 bins consists of 8 small TDCs with 8 bins. This is to reduce the workload of drawing the circuit schematic.

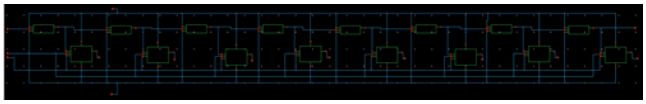

**Figure 8. Schematic of a TDC with 8 bins**

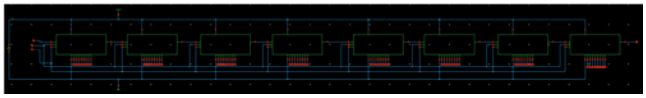

**Figure 9. The schematic of a 64-bin TDC, consisting of 8 8-bin TDCs**

## 3.4. The Voltage Sensor

The voltage sensor contains the voltage sensitive delay line and the TDC. A phase shifted clock signal first goes into the delay line and the output of the delay line is then used as the input to the buffer chain of the TDC. Thus the TDC converts the timing difference between the delay line output and the TDC clock signal into a sequence of binary digital code. The edge of the binary code indicates the delay and the delay further indicates the voltage level on the sensor. A schematic of the sensor is shown in Figure 10.

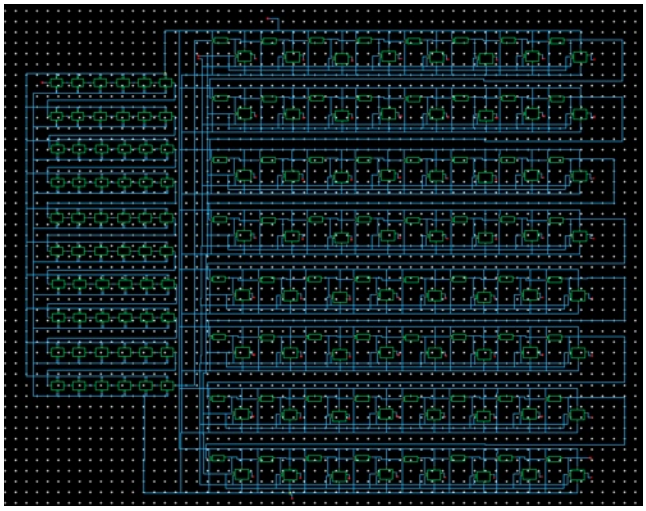

**Figure10. Schematic of the voltage sensor. Left side is the delay line and right side is the TDC.**

## 4. Simulation of the Sensor

The sensor is simulated in both static mode and dynamic mode. In static mode, the voltage level is fixed during the simulation and the static behavior of the sensor is evaluated. This is to verify the functionality of the sensor as well as to calibrate the sensor. In the dynamic mode, the power supply is modeled by a power network and the sensor is simulated as if it is in a real environment. The modeling power network can generate voltage transients and the sensor's response to voltage transients is evaluated.

## 4.1. Modeling the Power Network

In order to simulate the sensor, voltage transients need to be generated in the power network. There is a need to model the power supply and create a simulation environment that is as real as possible. In a real circuit, the power rails have resistance, inductance, and capacitance. The power rails are connected to loads, which causes current changes. The current changes further cause voltage changes in the power supply due to the inductance of the circuit according to the $L\frac{di}{dt}$ relationship. In the simulation, the loads are modeled as a current source, which is a current pulse with certain frequency and amplitude. The modeled power supply network is shown in Figure 11.

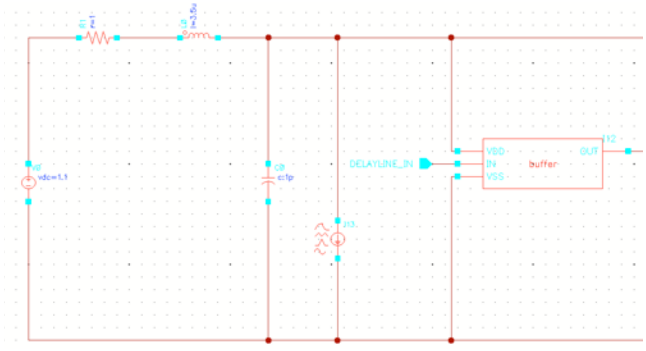


**Figure 11. Modeling the power supply.**

A simulation of the modeled power supply is shown in Figure 12. Changing the values of the resistance, inductance and capacitance

will change the power supply fluctuations. Generally, higher inductance produces more evident voltage transients.

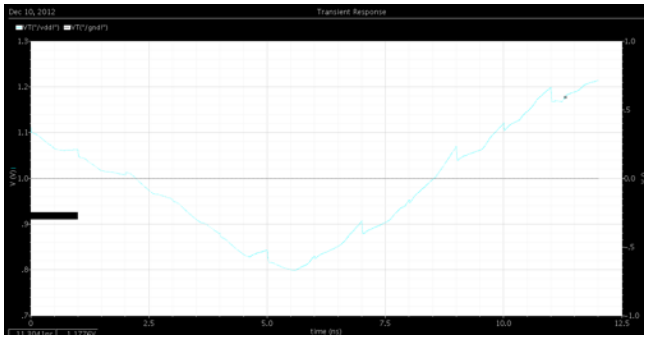

**Figure 12. Simulation of the power supply.**

## 4.2. Simulation Results

We simulated the sensor using the 45nm FreePDK library. The schematic of the sensor was created the simulation was done in the Spectre simulator. We first performed a static simulation where the voltage level is fixed during the simulation in order to verify the functional correctness of the sensor. The delay of the voltage sensitive delay line was simulated first and the results are shown in Table 5. As can be seen from the simulation results, the delay of the delay line is not equal at the high voltage end and at the low voltage end. The delay line is more sensitive to voltage changes when the voltage is low, while it is less sensitive to voltage when the voltage is high. This means that when calibrating the sensor, some correction should be made to compensate for this.

**Table 5. Static simulation results of the voltage sensitive delay line.**

| delay line with 100 open latches | | | | |
|---|---|---|---|---|
| **voltage (V)** | **rising time (ns)** | **falling time (ns)** | **tp (ns)** | **delay/voltage (ns/100mV)** |
| 0.7 | 4.717 | 4.707 | 4.712 | 0.46763 |
| 1.1 | 2.828 | 2.855 | 2.8415 | |
| 1.5 | 2.334 | 2.326 | 2.33 | 0.29775 |

Similarly we also performed a static simulation on the TDC. In the simulation, the edge of the output digital code can be clearly seen located between bin48 and bin49, as shown in Figure 13, and the edge shifted with the change of the voltage level, as shown in Table 6. The edge shift of the binary digital code is caused by the sensitivity of the delay of the buffer to voltage. However, the sensitivity of the buffer is much less than the open latch, thus it could not satisfy our design goal of the resolution and we need an extra voltage sensitive delay line to increase the sensitivity of the sensor to voltage changes. A simulation that combines both the delay line and the TDC shows that the sensor is too sensitive to voltage with 100 open latches, and the sensor can easily overflow or underflow with small amount of voltage changes. Accordingly, we reduce the number of latches in the delay line to 60, which gives a resolution around 1bin/10mV.

**Figure13. Simulation of the TDC. The edge of the binary digital code can be clearly seen.**

**Table 6. Edge shift of the binary digital code in TDC and its sensitivity to voltage changes.**

| Delay of TDC | | | |
|---|---|---|---|
| **voltage (V)** | **transition bin** | **No. of shift bins** | **bin/voltage** |
| 0.7 | 23,24 | 14 | 1bin/29mV |
| 1.1 | 37,38 | 0 | |
| 1.5 | 43,44 | 6 | 1bin/67mV |

A static simulation is also performed on the voltage sensor. The sensor now contains 60 open latches in the voltage sensitive delay line and a TDC which outputs 64-bit binary digital code. In the static simulation, the resolution of the sensor is evaluated and the edge of the binary code is recorded at different voltage levels. The sensor in the simulation has a measuring range from 0.9V to 1.5V. The sensitivity of the sensor around the nominal voltage is around 1bin/10mV, but the sensitivity increases as the voltage goes lower and decreases as the voltage goes higher. Thus a correction table is needed when interpreting the digital code. The input to the delay line is a phase shifted clock signal. In this simulation, the range of the sensor is closer to the higher voltage end, and this can be changed by changing the phase shift of the input signal to the delay line.

**Table 7. Edge shifting and sensitivity of the sensor.**

| **voltage (V)** | **transition bin** | **No. of shifted bins** | **bin/voltage** |
|---|---|---|---|
| 0.9 | 0,1 | 16 | 1bin/6.25mV |
| 1.0 | 16,17 | 13 | 1bin/7.69mV |
| 1.1 | 29,30 | 0 | |
| 1.2 | 39,40 | 10 | 1bin/10mV |
| 1.3 | 48,49 | 9 | 1bin/11mV |
| 1.4 | 56,57 | 8 | 1bin/12.5mV |
| 1.5 | 63,64 | 7 | 1bin/14mV |

In addition to the static simulation, we also performed a dynamic simulation on the voltage sensor. In the simulation, the sensor can effectively sense the voltage fluctuations, as reflected by the edge shift of the binary digital code. The simulation waveform is shown in Figure 14. The figure shows that the edge of the binary digital code shifts from bin22 to bin1 to bin10 and to bin35, indicating a dropping voltage followed by a rising voltage. This verified the functional correctness of the voltage sensor. The maximum sampling frequency of the sensor is determined by the delay of the

buffer chain in the TDC, and the maximum sampling frequency is calculated as 467MHz in the 45nm technology library.

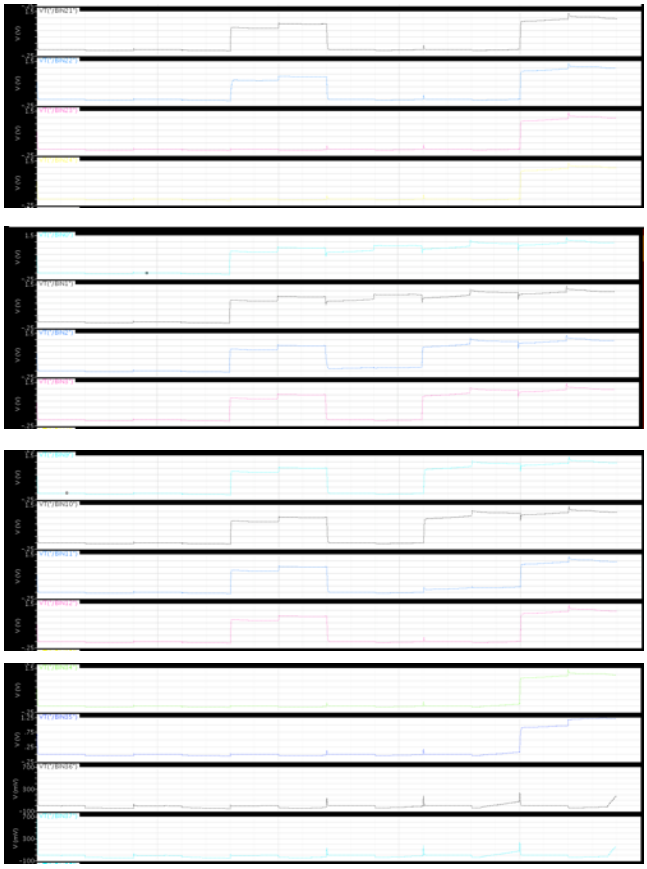

**Figure 14. Simulation waveform of the voltage sensor.**

## 4.3. Layout

In addition to the schematic, we did a layout of the sensor. The layout has passed the design rule check, and the layout verses schematic check. The parasitics of the layout was also extracted, providing data needed in the post-layout simulation. A picture of the layout is shown in Figure 15. The left side is the voltage sensitive delay line and the right side is the TDC.

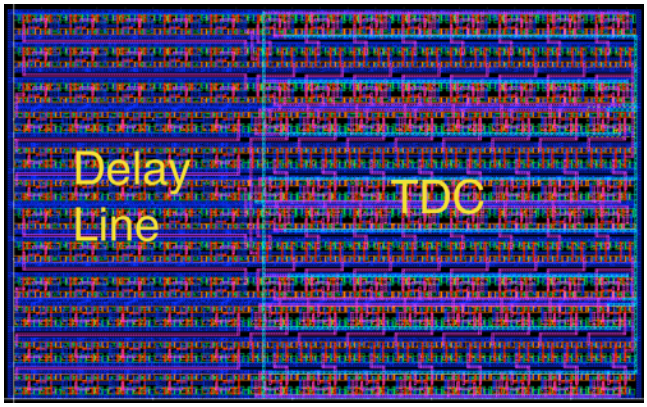


**Figure 15. Layout of the voltage sensor.**

## 5. Conclusions

In this work, the design of a novel purely digital voltage sensor is presented and evaluated. We investigated the voltage delay relationship of three basic delay gates and designed the voltage sensor. Our simulation has verified the correctness of the design. The sensor can effectively sense the voltage fluctuations at a speed of 467MHz and has a resolution of 1bin/10mV under nominal voltage. These number are get with the 45nm FreePDK library. With this sampling frequency, the sensor is capable of sensing any voltage transients that are longer than 2.14ns. The voltage sensor can be used in modern digital ICs to monitor the voltage safe margin or in security system to detect any voltage glitch related attacks.

## 6. Acknowledgments

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